University of Dayton

ECE

Mumma Radar Lab

Comprehensive VHDL

Fall 2016

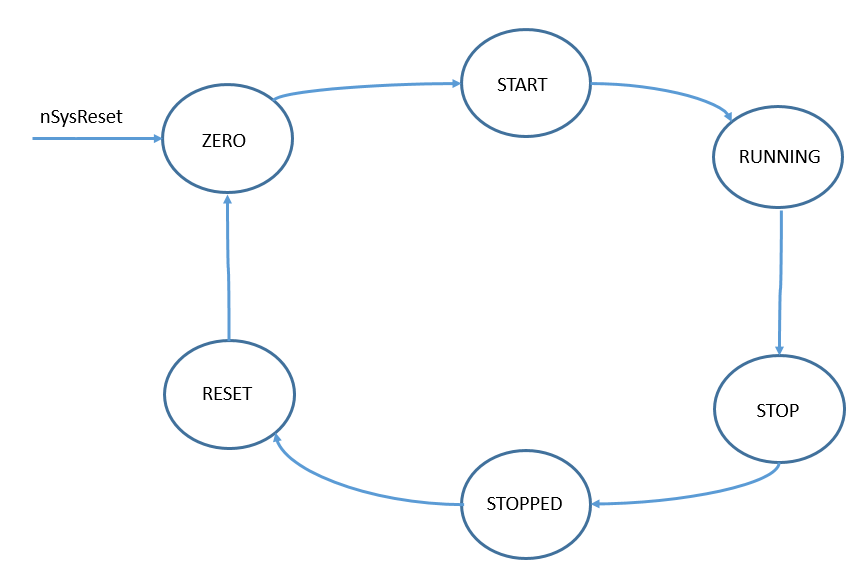
Homework 4

Finite State Machine

Electronic Stopwatch Controller



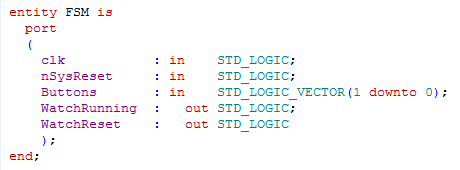
In this homework you will be designing Electronic Stopwatch Controller. You will be designing the following FSM diagram to control Electronic Stopwatch Controller:



You should have at least 6 states:



Here is the controller’s entity:



**The inputs:**

**Clk**: Use 100 MHz for the system clock.

**nSynsReset**: The system reset. It is active LOW, [it should take FSM to ZERO state].

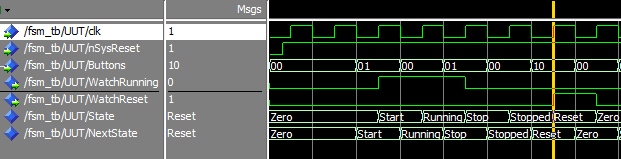
**Button**: Active high, when Button(0) is ‘1’, it should start or stop running the watch [FSM should be at START or STOP state]. When Button(1) is ‘1’ , it resets the watch to zero [FSM should go to ZERO state].

**The outputs:**

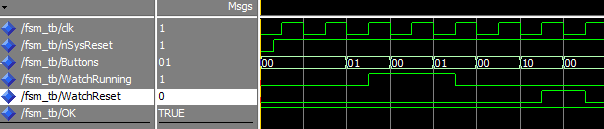
**WatchRunning**: active high, to control start and stop of the watch. When the user presses the start/stop button, this signal should go high for the watch to run [FSM in start state], and when the user presses the start/stop button again, this signal should go low [FSM in stop state] to stop the watch from running.

**WatchReset**: Active high. When this signal is high, the watch should reset to Zero

The RTL simulation should look like:



The TB simulation should look like:



Make sure you testbench should be self-check. Use something like:

